WHAT IS CLAIMED IS:

1. An information processing system comprising a plurality of host systems each having resources including a plurality of instruction processors and a plurality of memory segments, wherein

each of said host systems has a system status monitering and change instructing mechanism for managing statuses of said resources by a status management table, and

said system status monitering and change instructing mechanism has means for instructing an enhancement or reduction of an ability of a self host system in accordance with said status management table in accordance with a load that is applied to the self host system.

2. A system according to claim 1, wherein said system status monitering and change instructing mechanism has means for instructing the enhancement of the ability using the resources of another host system in accordance with said status management table in accordance with the load that is applied to the self host system.

3. A system according to claim 1, wherein said system status monitering and change instructing mechanisms of said host systems are mutually connected, arbitrary two host systems which establish a mutual hot standby have a first resource for an ordinary operation of the self host system and a second resource for hot

standby to another host system, use said first resource at the time of the ordinary operation, and use said second resource upon hot standby switching.

4. A system according to claim 3, wherein said arbitrary two host systems which establish the mutual hot standby have a third resource which can be allocated at the time of said ordinary operation and at the time of said hot standby switching.

5. An information processing system comprising a plurality of host systems which mutually independently operate and include instruction processors and memory segments and in which there is a surplus in the resources, wherein

each of said host systems has a system status monitering and change instructing mechanism which is physically independent of other component elements in said relevant host system and has an operating status management table of said resources, and each of said host systems has a function for automatically enhancing or reducing an ability of a self host system in accordance with said status management table in accordance with a load that is applied to the self host system.

6. A system according to claim 5, wherein said system has a function for enhancing or reducing the ability by using the resources of another host system in accordance with said status management table in

accordance with the load that is applied to the self host system.

7. A system according to claim 5, wherein said system status monitering and change instructing mechanisms of said host systems are mutually connected, arbitrary two host systems which establish a mutual hot standby have a first resource for an ordinary operation of the self host system and a second resource for hot standby to another host system, use said first resource at the time of the ordinary operation, and use said second resource upon hot standby switching.

8. A system according to claim 7, wherein said arbitrary two host systems which establish the mutual hot standby have a third resource which can be allocated at the time of said ordinary operation and at the time of said hot standby switching.

9. A system according to claim 5, wherein each of said host systems is connected to a remote console for integratedly managing all of the host systems, and each of the host systems has a function for setting a threshold value for said automatic enhancement or reduction in response to an instruction from said remote console.

10. A control method for an information processing system having a plurality of instruction processors and a plurality of memory segments, comprising the steps of:

setting an upper limit value and a lower limit value of a mean use rate of said plurality of instruction processors as a stable operating range;

activating the inactive instruction processors when said mean use rate of said instruction processors exceeds said upper limit value during the operation; and

inactivating the active instruction processor when said mean use rate of said instruction processors is lower than said lower limit value during the operation.

11. A method according to claim 10, further comprising the steps of:

setting an upper limit value and a lower limit value of the mean number of paging occurrence times of said plurality of memory segments as a stable operating range;

activating the inactive memory segments when said mean number of paging occurrence times of said memory segments exceeds said upper limit value during the operation; and

inactivating the active memory segment when said mean number of paging occurrence times of said memory segments is lower than said lower limit value during the operation.